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MEETING YOUR TESTING NEEDS TODAY AND TOMORROW

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APPLICATION NOTE

T1 Test Patterns

INTRODUCTION

A number of patterns are available for testing T1 circuit performance. This inevitably leads to the questions: “Which pattern should I use?” and “What does it mean when the circuit fails a bit-error-rate-test (BERT) on one pattern but passes another?” The following article is a brief discussion of the test patterns found in today’s T1 test sets and the use of each pattern.

GENERAL USAGE

A T1 test pattern is a predetermined bit sequence in the DS-1 data. These patterns are designed to stress T1 equipment or to simulate customer data traffic. Stress patterns cause the equipment to operate at the limits of specifications regarding consecutive zeros, ones density and line coding. Traffic simulation patterns attempt to simulate the random nature of customer traffic.

The ANSI standard for T1 transmission requires an **average** ones density of 12.5% (a single one in eight bits meets this requirement) with no more than 14 consecutive zeros for unframed signals and no more than 15 consecutive zeros for framed signals. The primary reason for enforcing a ones density requirement is for timing recovery or network synchronization. However, other factors such as automatic-line-build-out (ALBO), equalization, and power usage are affected by ones density.

Line coding for T1 signals is either alternate mark inversion (AMI) or bipolar eight zero substitution (B8ZS). B8ZS is introduced on a circuit to ensure that the 12.5% ones density requirement is always met. B8ZS is actually an AMI encoded circuit that has the addition of a unique code whenever the transmitted signal contains eight zeros in a row. Thus, a B8ZS circuit will appear to be optioned as AMI unless the signal meets the eight consecutive zeros requirement. Another consideration is that not all equipment in a B8ZS circuit will inject a B8ZS code. As an example, line repeaters typically do not enforce the B8ZS code and simply pass whatever signal they receive. Due to the difference in consecutive zeros, a pattern may fail if the test point is on the “span side” using AMI encoding but pass if transmitted from a central office or end point where B8ZS is used. This situation would indicate that the circuit will probably work for customer traffic as long as the B8ZS encoding is maintained, however, the circuit is marginal, at best, and will not be suitable for AMI encoding.

Customer traffic is simulated by sequences that contain “all” bit patterns up to a specified length. These test patterns are pseudorandom, and not truly random, to allow test sets to recognize the pattern and synchronize to it.

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COMMON PATTERNS

3 in 24

This is a 24 bit pattern which contains three (3) ones. The longest string of consecutive zeros is fifteen (15) and the average ones density is 12.5%. This pattern is used primarily to test timing (clock) recovery and may be used framed or unframed for that purpose. This pattern will force a B8ZS code if transmitted through equipment optioned for B8ZS*.

1:7 (also written as 1 in 8)

This is an eight (8) bit pattern which contains a single one. This pattern is used primarily to test timing (clock) recovery and may be used framed or unframed for that purpose. When transmitted unframed the maximum number of consecutive zeros is seven (7) and the pattern will not force a B8ZS code. When transmitted framed, framing bits force the maximum number of consecutive zeros to eight (8), and the pattern will force a B8ZS code from equipment optioned for B8ZS.*

QRSS

This pseudorandom sequence is based on a twenty (20) bit shift register and repeats every 1,048,575 bits. Consecutive zeros are suppressed to no more than fourteen (14) in the pattern and it contains both high and low density sequences. QRSS is the most commonly used test pattern for T1 maintenance and installation. This pattern will stress timing recovery, ALBO and equalizer circuits, but it also simulates customer traffic on the circuit. The QRSS pattern can be used framed or unframed and will force a B8ZS code in circuits optioned as B8ZS.*

ALL ONES

This pattern is composed of ones only, and causes line driver circuity to consume the maximum amount of power. In a circuit with repeaters, this pattern will verify that the dc power is regulated correctly. When transmitted unframed, an all ones pattern is defined in some networks as an Alarm Indication Signal (AIS). An unframed all ones signal may also be referred to as a “Blue Alarm”and is sent forward by a device that has lost its input signal. Framed all ones is often used as an idle condition on a circuit that is not yet in service. Thus, all ones is the most common pattern found on a circuit during installation. This pattern **will not** have a B8ZS code present, even if the circuit is optioned for B8ZS.

ALL ZEROS

This pattern is composed of zeros only and must **only** be used on circuits optioned for B8ZS. The pattern verifies that all circuit elements are optioned for B8ZS and should be used whenever a B8ZS circuit is under test.

T1-DALY and 55 OCTET

Each of these patterns contain fifty-five (55), eight (8) bit octets of data in a sequence that changes rapidly between low and high density. These patterns are used primarily to stress the ALBO and equalizer circuity but they will also stress timing recovery.
55 OCTET has fifteen (15) consecutive zeros and can only be used unframed without violating ones density requirements. For framed signals, the T1-DALY pattern should be used. Both patterns will force a B8ZS code in circuits optioned for B8ZS*.

OTHER PATTERNS

2 in 8

This is an eight bit pattern with two ones and a maximum of four consecutive zeros. It can be used either framed or unframed and will not force a B8ZS code. It is sometimes used on AMI circuits which have errors on QRSS or 3 in 24 patterns. If used in this manner and no errors occur, it is an indication of the possible presence of a device optioned for B8ZS in a circuit that should be AMI only. See MULTIPLE under Test Pattern Sequences.

T1-1 (MIN/MAX)

This pattern consists of 72 octets that generate rapid transitions from low ones density octets to high ones density octets. It is commonly used to test preamplification, equalization and ALBO circuitry.

T1-2 (TRIP TEST)

This is a 96 octet pattern that generates a long series of high ones density octets followed by rapid changes from average ones density to low density octets. It is commonly used to detect faulty multiplexing circuitry in DS-3 equipment.

**Note: When a B8ZS code is injected into a test pattern that contains a long string of zeros, the pattern is no longer testing to the full consecutive zero requirement. Circuit elements, such as line repeaters, that are intended to operate with or without B8ZS should be tested without B8ZS.*

T1-3 (54 OCTET)

This is a 54 octet pattern used to test pre-amplification, ALBO and equalization circuitry. It consists of 54 octets with rapid transitions from low ones density octets to high ones density octets.

T1-4 (120 OCTET)

This is a 120 octet pattern that consists of rapid changes from high ones density to minimum ones density. It is sometimes used to stress the equalization circuits of T1 multiplexers.

T1-5 (53 OCTET)

This pattern consists of 53 octets that generate rapid transitions from low ones density octets to high ones density octets. It is commonly used to test pre-amplification, equalization and ALBO circuitry.

T1-6 (55 OCTET)

This is the 55 OCTET pattern discussed in the COMMON PATTERNS section.

CHANNEL TEST PATTERNS

These patterns should not normally be used to test T1 services because they violate ones density and/or consecutive zeros restrictions for T1 signals. However, they may be used to simulate customer traffic for testing a channel (DS-0), in a Drop/Insert mode, or in certain cases for “gateway” testing to an E1 (2048Kb/s) network.

2047

This pseudorandom sequence is based on an eleven (11) bit shift register.

2E15-1

This pseudorandom sequence is based on a fifteen (15) bit shift register.

2E20-1

This pseudorandom sequence is based on a twenty (20) bit shift register.

2E23-1

This pseudorandom sequence is based on a twenty-three (23) bit shift register.

FOX

This is an ASCII text message consisting of all letters and digits. “THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 1234567890”.

DDS PATTERNS

DDS patterns are primarily intended to test Digital Data Service (DDS) circuits, which are data services of 64Kb/s or less, when delivered to a customer. These patterns are not suitable for use in testing the T1 service, but are used on a T1 channel (DS-0) in a Drop/Insert mode to test the DDS service when test access is on a T1.

DDS-1

This is a 200 octet pattern that consists of 100 octets of all ones followed by 100 octets of all zeros. It is used to stress the signal recovery capability of DDS circuits.

DDS-2

This pattern is 200 octets consisting of 100 octets of 7EH (01111110) followed by 100 octets of all zeros. This pattern simulates bit oriented protocol flags for DDS testing.

DDS-3

This is a 16 octet pattern that provides a continuous stream of medium ones density octets. Each octet is 4CH (1001100). It is used to simulate a typical DDS signal.

DDS-4

This is a 16 octet pattern of low density octets. Each octet is 40H (01000000). It is used to stress DDS clock recovery.

DDS-5

This is a 2000 octet pattern that consists of 800 octets of DDS-1, 800 octets of DDS-2, 200 octets of DDS-3 and 200 octets of DDS-4. It is used as a quick test of DDS circuit operation.

DDS-6

This is an 8 octet pattern that consists of seven octets of FEH (11111110) followed by one octet of FFH (11111111). It is used to simulate the transition from IDLE mode to DATA mode in a DDS signal.

TEST PATTERN SEQUENCES

Q-TEST or QUICK TEST

This is a sequence of the patterns discussed in the Common Patterns section. Each pattern is executed for five (5) seconds and a PASS/FAIL indication is displayed. ALL ZEROS is only executed when the B8ZS option is set. The sequence is used to quickly verify the probability of the circuit passing a full conformance test which would typically take much longer to perform.

L-TEST or LONG TEST

This is identical to the Q-TEST sequence, but the execution time is selectable.

BRIDGE

This sequence is also called “BRIDGE TAP” and is used to detect the presence of a bridge tap on a circuit that has been converted from analog use. The sequence consists of twenty- one (21) patterns starting with ALL ONES and ending with QRSS. Each pattern is transmitted for 30 seconds and monitored for only 23 seconds. The results are reported for each individual pattern and on the entire sequence. The sequence has the effect of generating a series of “digital tones” to detect the resonance of the bridge tap. If present, the bridge tap will cause bit errors and bipolar violations in one or more of the patterns. **All B8ZS options must be “OFF” for this sequence to be effective in detecting the bridge tap.**

MULTIPLE

This sequence is sometimes called “Multi-Pat” and is used to perform acceptance testing of a new T1 span or for trouble shooting an existing span. It consists of five (5) patterns (ALL ONES, 1:7, 2 in 8, 3 in 24 and QRSS) where each pattern is transmitted for three (3) minutes and monitored for 175 seconds. The results are reported for each individual pattern and on the entire sequence.

CONCLUSION

No single test pattern provides exhaustive verification of a T1 circuit’s performance. A selection of test patterns is required to identify problems and assure that the network is operating within acceptable standards. At a minimum, the patterns discussed in the COMMON PATTERNS section should be used to verify each T1 circuit at installation and after repair. The use of a test sequence such as Q-TEST, L-TEST or MULTIPLE can greatly simplify the test procedure and reduce the over-all test time.

Regardless of the test pattern or sequence in use, the technician must be aware of the effect framing and line coding options have on the transmitted pattern and on the expected results. Proper pattern selection and interpretation will reduce test time and the need for repeat service calls.

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